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Effect of Electrical Forming on the Charge Impurity Distribution of Selenium Cadmium Diode

V T INGOLE AND A A GHATOL, FIETE
Department of Electronics and Telecommunication, Government College of Engineering,
Amravati 444 603, India.

The paper discusses the effects of electrical forming on selenium cadmium diode. It is reported that charge impurity (N_a) and reverse bias current (I_r) decrease due to electrical forming. The decrease in N_a is reported to be due to the decrease in mobile charge carriers in the depletion region. The rate of forming is higher at the junction and reduces at a distance from it. The changes in N_a, incremental shunt resistance (R_d) and width of depletion region (W_d) follow exponential trend with particular time constant. It is reported that forming does not change the immobile charge distribution in the present device.

Indexing terms: Electrical forming, Selenium device, Metal rectifier.

SELENIUM cadmium diode commercially known as selenium diode or rectifier is the very first semiconductor diode reported by F Braun in 1874 and was regarded as a metal semiconductor junction. Selenium diodes are used in battery charger, electroplating and excitation system for generator etc. The exact nature of such semiconductor junction and the effect of electrical forming on it, have been a subject of contoversy right from it's invention [1]. The electrical forming is unique to the selenium diode and is a very important part of manufacturing process. In order to improve the diode performance under reverse bias condition, it is necessary to form the device by passing rectified alternating current through it in the reverse direction for certain duration. The earlier investigation suggested that forming increased the barrier thickness [2]. Champness [3] suggested that electrical forming caused a reduction of the chlorine, or other deep acceptors, in a region about half a micron from the junction, probably due to field induced ion drift. He suggested that pure electrical forming did not create a CdSe layer thicker than 50Å whereas thermal forming did. The present investigation is directed towards finding out the exact mechanism of electrical forming so as to optimize the electrical forming duration.

In the present work, Se-Cd devices are fabricated by vacuum deposition technique with interfacial insulation layer. The effect of electrical forming time (EFT) on the impurity distribution, depletion width, incremental shunt resistance of the depletion region and their relations at different EFT intervals are studied.

FABRICATION

The selenium rectifier structure is fabricated as described in [4,5] for the present work and is shown in Fig 1. One micron thick Bismuth layer is vacuum deposited on the roughened side of aluminium base plate. Approximately 50 micron thick selenium layer, doped with 200 ppm chlorine (in the form of selenium tetrachloride) is vacuum deposited on the Bismuth layer. The interlayer Bismuth provides an ohmic contact. The surface of selenium is coated by a uniform layer of lacquer, by using a solvent spray technique. Lacquer consists of a solution of organic insulating materials in volatile solvents. The amorphous selenium is then subjected to crystallization by heat treatment. The substrate is kept at room temperature and a layer of tin and cadmium alloy (melting point 177° C) of approximately 60 micron thickness is coated on selenium by hot metal spray technique. The devices are further treated at 215° C for 30 minutes in an oven to form a semiconductor junction. In the device the selenium side acts as an anode and cadmium side acts as a cathode or a counter electrode. In order to avoid the change in device parameters due to material and process variation, the device having an area of approximately 1 sq cm, each are fabricated in batches and selected for the studies. In order to improve the performance of selenium rectifier under reverse bias condition, it is necessary to form the device by passing rectified alternating current in the reverse bias [2].

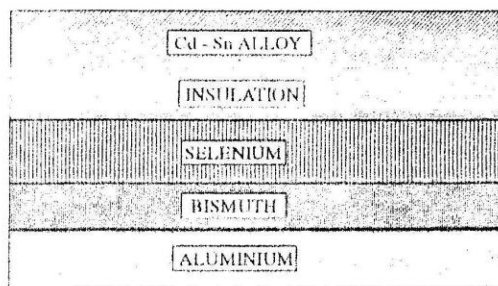

Fig 1 Cross-section showing the layer structure of Se-Cd diode

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MEASUREMENTS AND RESULTS

Experiments are carried out "before forming", and at interval of 0.5, 1.0, 1.5 and 4.5 hr EFT during electrical forming and measurements are carried out after each EFT interval. Measurements are coded as EF0, EF0.5, EF1, EF1.5 and EF4.5, where the number signifies the forming duration in hour(s).

The measurements of incremental depletion capacitance (C_i) and incremental shunt resistance (R_d) are carried out on one of the devices from the batch for EF0 to EF4.5 with the help of a capacitance bridge at different reverse bias voltages (V_r). Due care is taken to complete the measurements in shortest time to avoid dc creep in the device.

The experimental values of C_i are plotted against V_r for EF0, EF0.5 and EF4.5 in Fig 2. It is observed that C_i decreases with the increase in V_r, except in EF0 where C_i increases as opposed to the decrement at higher V_r.

Impurity distribution in the depletion region is evaluated by assuming a power law distribution as suggested by Norwood [6] which is given as,

$$N_a = N_0\, x^m, \quad \text{for } x > 0 \tag{1}$$

where, x = distance from the junction,

N_a = impurity charge density at x,

N_0 = impurity charge density at $x = 0$, and

m = grading exponent or impurity exponent.

By solving one dimensional Poisson's equation as suggested in [6], relation for C_i is obtained as,

$$C_i = A\,\{q\, N_0\, (\varepsilon)^{m+1} / [(m+2)(V_d + V_r)]\}^{1/(m+2)} \tag{2}$$

where A = area of junction,

q = charge of electron,

V_d = diffusion voltage,

V_r = reverse bias voltage, and

$\varepsilon = \varepsilon_0\, \varepsilon_r$ = dielectric permittivity.

The slope of $\ln(C_i)$ and $\ln(V_d + V_r)$ is known as capacitance exponent or sensitivity factor [6,7] and is given as,

$$S = -d\,[\ln(C_i)] / d\,[\ln(v)] \tag{3}$$

where S = sensitivity factor or capacitance exponent and

$$V = V_d + V_r$$

Solving equations 2 and 3 yields,

$$S = 1/(m+2) \tag{4}$$

The values of S are calculated from eqn (3) and plotted for V_r in Fig 3. It is observed that the values of S are nearly 1 near the junction. Equation 4 gives $m = -1$ for $n = 1$. By substituting value of m in eqn (1) we get

$$N_a = N_0\, x^{-1} \tag{5}$$

It is noted that the impurity distribution is hyperabrupt, as reported in [5,7]. At $x = 0$ the function becomes singular but the present analysis is carried out at $x > 0$ so the validity of the eqn (5) is conserved.

Combining eqns (2), (3) and (4), we get,

$$(1/C_i)^{1/S} = B\,(V_d + V_r) \tag{6}$$

where $B = (m+2) / \{A\,[q\, N_0\, (\varepsilon)^{m+1}]\}$

And for $S = 1$, eqn (6) becomes,

$$1/C_i = B\,(V_d + V_r) \tag{7}$$

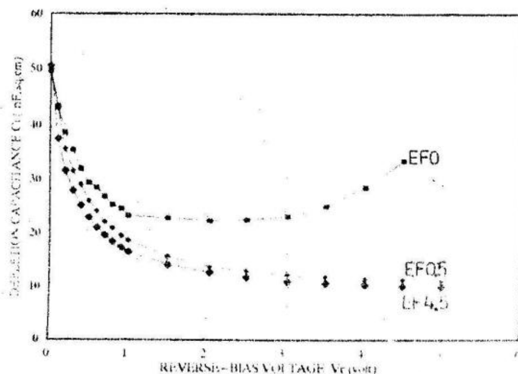

Fig 2 C_i *versus* V_r relation at different interval of electrical forming

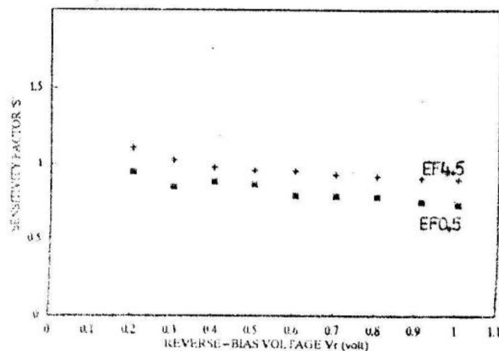

Fig 3 Effect of forming on sensitivity factor (S) at different reverse voltages

$1/C_i$ is calculated from experimental values and plotted against V_r in Fig 4. The relation is observed to be a straight line for different EFT intervals. Interpolation on abscissa gives the values of diffusion voltages (V_d) and are found to be −0.7 V and −0.6 V for EF0, EF4.5 respectively.

In order to find out impurity distribution from C-V, plot (Fig 2), the method as described in [8] is used where the values of N_a (assuming depletion region validity), for unit device area is given as,

$$N_a = 2\,(C_i^3/q\,\varepsilon)\,(dV_r/dC_i) \quad (8)$$

$$\text{and } W_x = \varepsilon / C_i \quad (9)$$

where W_x = distance from the junction.

Values of N_a and W_x are calculated from eqns (8) & (9) for different EFT and plotted in Fig 5. From the nature of the curve, it is apparent that the junction is hyperabrupt. It is further observed that N_a plot shifts downward with increase in EFT. It suggests that impurity decreases with EFT without affecting the nature of the profile or impurity exponent ($m = -1$). In case of EF0, N_a decreases up to W_x = 0.35 micron, and then starts increasing at an abnormally high rate. Similar deviation is also observed for EF4.5 at $W_x > 0.6$ micron but at a lower rate. It is further observed that N_a profiles for EF0.5, EF1, EF1.5 and EF4.5 appear to merge at higher W_x.

Maximum depletion width (i.e., max $W_x = W_d$), is calculated from eqn (9) and plotted for V_r at different EFT intervals in Fig 6. The increase in W_x is at a higher rate for lower V_r but the rate decreases at higher V_r. However for EF0 W_d starts decreasing abnormally for $V_r > 2.5$ volts as opposed to other characteristics.

Experimentally measured R_d is plotted against V_r for different EFT in Fig 7. It is observed that R_d increases progressively with EFT. For EF0.5 and EF4.5, it is observed that R_d increases at a higher rate for lower V_r

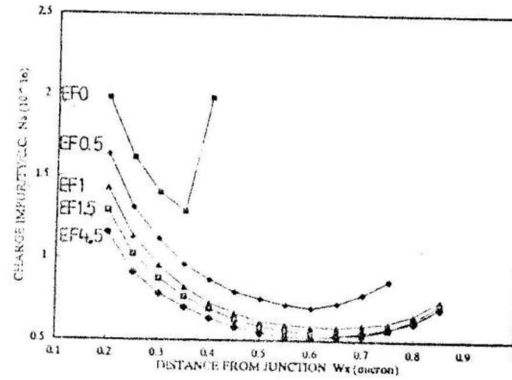

Fig 5 Plot of density of charge impurities as a function of distance from the junction at different intervals during forming

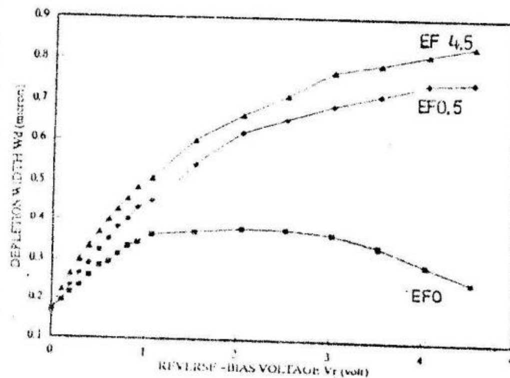

Fig 6 Effect of electrical forming on the depletion width at different reverse voltages

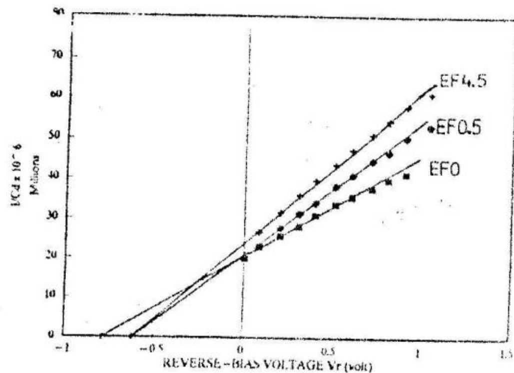

Fig 4 Effect of electrical forming on diffusion voltage (V_d) by ($1/C_i$) against reverse voltage plot

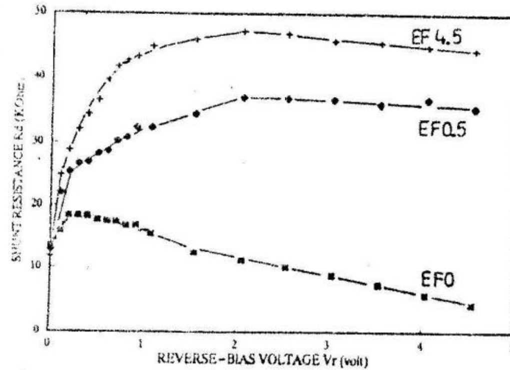

Fig 7 Variation of incremental shunt resistance as a function of reverse voltage at different intervals during forming

whereas at lower rate for higher V_r. Interestingly for EF0 after the initial rise of R_d, it starts decreasing at higher V_r as opposed to other observations. This may be due to generation of large mobile carriers because of depletion region breakdown. Point defects are known to affect resistance and cause such an early breakdown [9]. Such defects may probably be present due to lack of "forming". This further suggests that the depletion region is not ideal.

Diode current as given in [8] is expressed as,

$$I = I_s [1-(V/V_d)] [\exp(-V/a V_T) - 1] \quad (10)$$

and

$$I_s = [q A R^* T V_d / K] \exp(-V_d / a V_T) \quad (11)$$

where I_s = thermal current,

V_T = KT/q,

a = ideality factor,

R^* = Richardson constant,

T = absolute temperature in degree Kelvin,

K = Boltzman constant, and

V = Voltage across the diode.

From eqns (10) & (11) we get,

$$I = [q A R^* T/K] \exp(-V_d/V_T) (V_d - V) [\exp(-V/a V_T) - 1] \quad (12)$$

For $V = -V_r$ and $V_r > 4\ V_T$ then $I = -I_r$ and eqn (12) reduces to,

$$I_r = -(V_d + V_r)/R_d \quad (13)$$

where I_r = reverse bias current, and

$$1/R_d = [q A R^* T/K] \exp(-V_d/V_T)$$

In order to find out the co-relation of reverse bias current I_r (eqn (13)) and N_a at W_x (eqn (9)) the relevant quantitites are calculated and plotted in Fig 8. It is observed that for EF0 at W_x = < 0.35 micron and for EF4.5, at W_x = < 0.75 micron, I_r increases linearly and N_a decreases normally. However in both the relations, at higher values of W_x, the bias currents increases at higher rates, associated with abnormal increases in N_a. Such concurrent relations between I_r and N_a suggest that the reverse bias current (mobile charge carriers), influences the N_a profile. This further suggests that the values of N_a (eqn (8)) consists of both immobile (ionized) and mobile charge carriers. Thus the decrease in N_a is caused because of the reduction of the mobile charges in the depletion region on account of electrical forming.

C_i and R_d can be expressed in terms of depletion region dimentions as:

$$C_i = \varepsilon A/W_d \quad (14)$$

and

$$R_d = W_d / A\ \sigma \quad (15)$$

where σ = conductivity

On multiplication of eqns (14) and (15) we get,

$$\sigma = \varepsilon / (C_i R_d) \quad (16)$$

The σ is thus calculated from eqn (16) from experimental values of C_i and R_d for different EFT intervals at fixed V_r and plotted against V_r in Fig 9. It is observed that the electrical forming does not change the conductivity at V_r = zero voltage. It is probably due to ongoing action of built in voltage. It is further observed that σ increases with increase in V_r and also progressively decreases with EFT. The changes in σ are more pronounced in EF0 than in EF4.5. It is known that the diffused metallic impurities dominate the conduction mechanism of the depletion region by increasing the mobile charges. It appears from these relations that during forming such impurities might

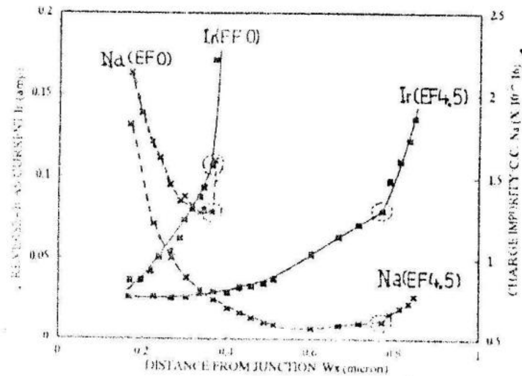

Fig 8 Co-relation between reverse bias current and density of charge impurity as a function of distance from the junction, before and after forming

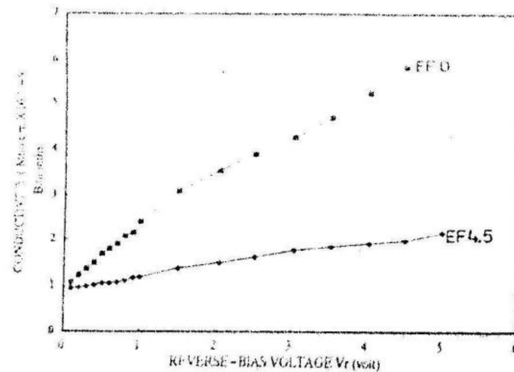

Fig 9 Change in conductivity, before and after forming, as a function of reverse bias voltage

be diminishing due to bonding of Cd and Se thereby reducing the mobile charge generation centres (point defect).

In order to understand the field-induced drift mechanism values of R_d, W_d and N_a were compiled for EF0 through EF4.5 at different V_r. R_d and W_d against EFT intervals for different V_r are plotted in Figs 10 & 11 respectively. N_a against EFT at $W_d = 0.2$ micron is plotted in Fig 12. Variation of R_d, W_d and N_a against EFT is exponential as apparent from Figs 9,10 & 11 and governed by certain time constants. The time constant may be influenced by the manufacturing process. Further observation of Figs 9,10 suggests that the time constants for R_d & W_d are similar at same V_r. Observation of Fig 12 also suggests that the reduction in N_a follows an exponential trend. From the above observations it appears that the process of "forming" is faster at the junction than at away from it. It may probably be due to field-induced drift as it is known to be higher at the junction than at away from it [10].

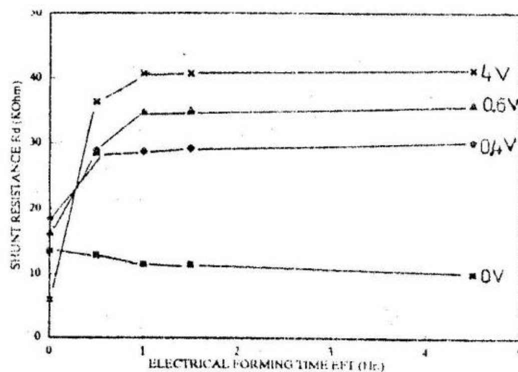

Fig 10 The increment in R_d as a function of forming time computed at different V_r

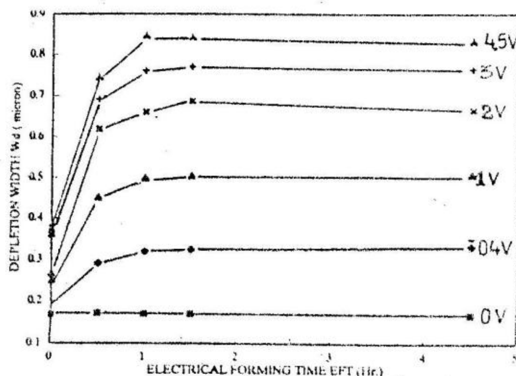

Fig 11 Growth of depletion region (W_d) as a function of forming time computed at different V_r

DISCUSSION

It appears from the observations that the ionized or immobile impurity does not seem to be affected by electrical forming as the nature of impurity profile ($m = -1$) remains unchanged. Since R_d is related to I_r and in turn to mobile charge carriers nq, the increase in R_d accounts for a decrease in nq, thus implying that electrical forming decreases nq. The mobile charge impurities nq appear to be related to point defects. The cadmium may diffuse in the selenium lattice during the fabrication and form point defects. Such point defects are known to change the resistance of the semiconductor [9]. The observations of R_d and σ suggest that the electron-hole generating sources within the depletion region are being depleted during the course of forming. Due to field-induced drift the point defect formed by metallic cadmium gets bonded to selenium ion to form CdSe thus ceasing to be a point defect any more. Thus the forming may be interpreted as a process of converting metallic impurities in to either a chemical compound or charge transfer complex [11] of Cd and Se.

It is further suggested that the process of forming depends upon the electric field, drift velocity and forming duration. It is known that in the depletion region maximum electric field exists at the junction and it reduces away from the junction and so the drift velocity chances according to the electric field. It is also known that CdSe has a co-valent bond which is weaker than an ionic bond [10]. For the formation of such bond, it is imperative for Cd and Se ions to get close enough by either drift or diffusion so that electrostatic coulomb force can interact with ions. Ion migration time will depend upon the drift velocity and will be shorter near the junction than at a distance away from it. Thus the forming near the junction is faster than at the depletion region boundary. Thus it may be inferred that electrical forming reduces the mobile charge carriers due to field-induced

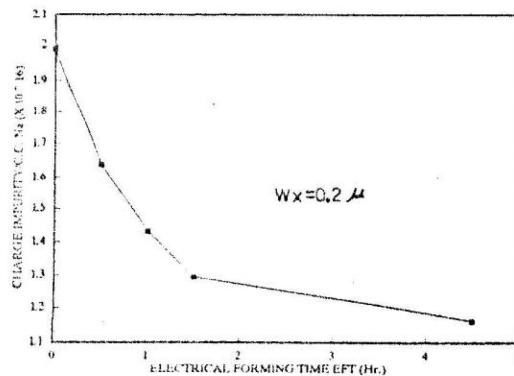

Fig 12 Density of charge impurity at a distance of 0.2 micron from the junction, plotted against the electrical forming time

drift, forming voltage, EFT, the location (W_x) & density of the metallic impurites.

From the above discussions, in a selenium device the electrical forming process as a whole may possibly (Fig 11) progress in the manner as described below.

Immediately after the fabrication the process of diffusion starts across the junction and the depletion region is formed. Diffused Cd occupies vacant sites in the selenium layer creating point defect. Point defects generate mobile charges on application of forming voltage. The forming voltage sets up electric field across the depletion region which is highest at the junction and lower at a distance away from it. The metallic impurities drift under the influence of field till Selenium ions are encountered. The coulomb forces between the two ions leads to the formation of co-valent bond and thus point defects are trapped. The reduction of mobile charges due to reduction in point defects increases R_d and W_d. The increased W_d encompasses new impurities from the hitherto neutral selenium region. Thus the process of electrical forming commences in the new region of Se layer, though at a reduced rate due to lower drift velocity. Higher forming voltage (which is increased following the drop in forming current) will cause an additional increase in W_d and the forming would extend further in the depletion region (at higher W_x). This process may continue till the depletion region is void of point defects and would require particular time. It is known that when device is not in service or is used in lower voltage application for a long time, it tends to lose some of its forming [12]. It appears that CdSe bond may be less stable in electrically formed device. Absence or weak electric field may lead to the dissociation of weak CdSe bond or charge transfer complex formed by electrical forming due to lattice vibrations in the absence of electric field. This explanation may throw some light on the anomalies of the device such as creep, memory effect.

CONCLUSION

The electrical forming causes field-induced drift of cadmium defects on selenium side leading to the formation of CdSe bond. The electrical forming does not appear to decrease the ionized impurity distribution. It reduces the excess charge carrier due to reduction of generating sources by bonding the free metallic cadmium impurity which may be in the form of Cd-Se charge transfer complex. Electrical forming process is exponential in nature and depends upon the forming voltage, electric field, forming duration and density & location of Cadmium impurities in Selenium layer.

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