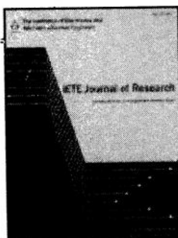

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Effect of Post Thermal Treatment on the Impurity Charge Distribution of Selenium Cadmium Diode

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The paper discusses the effect of post thermal treatment on impurity charge distribution of Selenium Cadmium diode. It is reported that the thermal treatment affects the impurity distribution profile near the junction. Abrupt, graded and hyperabrupt profiles are developed by thermal treatment at 35° C, 130°C and 215°C respectively.

Indexing terms: Selenium rectifier, Metal rectifier, Thermal forming.

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SELENIUM Cadmium diode, commercially known as Selenium rectifier, is the very first semiconductor device reported by F Braun in 1877. The exact nature of such semiconductor junction has been a subject of contradiction right from its invention. It was regarded as a metal-semiconductor diode and later on suggested to be a heterojunction of n-type CdSe and p-type selenium. Likewise the heat treatment has been regarded as a process of combination of Cadmium and selenium to form a cadmium selenide compound. In the literature the junction has generally been referred to as an abrupt junction[1-3], though it does not seem apparent. Selenium diodes are much more robust and known for their reliability. In certain applications such as battery chargers, electroplating equipments, excitation systems for generators etc selenium diode, due to it's self healing properties[4], cannot be effectively substituted by silicon diode. Selenium diode can be fabricated with large junction area thereby large values of depletion capacitance can be easily realized. In case of low to very low frequency tuning applications, such parameter of selenium diode could be effectively exploited, however it is desirable for such devices to have hyperabrupt impurity profile.

The present study reports the effect of thermal treatment on the impurity distribution. It is known that diffusion depends on thermal treatment and perhaps change the impurity distribution, hence devices are fabricated with vacuum deposition technique with inter facial insulation layer and treated at different temperature for the present study.

FABRICATION

The selenium rectifier structure, fabricated generally as described in[4] for this work is as shown in Fig 1. One micron thick bismuth is vacuum deposited on the roughened side of aluminium base plate. Approximately 50 micron thick selenium, doped with 200 ppm chlorine (in the form of selenium tetrachloride) is vacuum deposited on the bismuth layer. The inter-layer bismuth provides an ohmic contact. The surface of selenium is coated by a uniform layer of lacquer, by using a solvent spray technique. Lacquer consists of a solution of organic insulating materials in volatile solvents. The amorphous selenium is then subjected to a crystallization by heat treatment. The substrate is kept at a room temperature and a layer of tin-cadmium alloy (melting point 177°C) of approximately 60 micron thick is coated on selenium by hot metal spray technique to form a rectifying junction. In the device the selenium side acts as an anode and cadmium side acts as a cathode or a counter electrode. Devices each of an area of 1 sq cm are fabricated in batches for the present study and selected for further treatments by dividing the devices in 5 groups.

The selection of thermal treatment is decided on the diffusion process as it is known to depend on treatment time, temperature and melting points (MP) of the elements.

One group is not given a post thermal treatment and studied at 35°C room temperature (35/0), the second group is treated below the melting point of cadmium alloy and selenium (MP 217°C) at 130°C for 90 minutes (130/90). The third, fourth and fifth groups are treated at 215°C, at which Cd alloy is in molten state and Se is near to its melting point, for 30 minutes (215/30), 60 minutes (215/60) and 90 minutes (215/90) respectively and coded as per the bracketed numbers respectively.

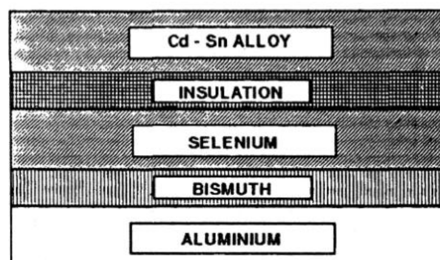

Fig 1 Cross section showing the layer structure of selenium cadmium diode

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MEASUREMENTS AND RESULTS

In order to improve the diode performance, under reverse bias condition, it is necessary to "form" the device by passing rectified alternating current in the reverse direction for a number of hours, such that when the reverse characteristic improved, the applied voltage is increased till such time after which there is no further decrease in the reverse bias current[3]. Measurements on the devices are carried out before forming and after forming.

It is noted that the forming time generally decreases with higher treatment temperature and duration.

Incremental depletion capacitance C_i and incremental shunt resistance R_d measurements of the devices are carried out with the help of a capacitance bridge before forming and also after forming, for different reverse bias voltages (V_r). Due care is taken to complete the measurement in a shortest possible time to avoid dc creep in the devices.

Following observations are made on formed devices. C_i *versus* V_r is plotted in Fig 2. It is observed that C_i continuously decreases with increase in V_r for all devices. It is further observed that the change in C_i is lowest for 130°C temperature treatment (130/90) and highest for 215°C (215/90).

In order to find out impurity distribution and C_i, a power law distribution is assumed as suggested by Norwood in[5], which is given as,

$$N_a x = N_o x^m \quad (1)$$

where $x > 0$,

x = distance measured from the junction,

N_a = impurity density,

N_o = impurity densitiy at $x = 0$, and

m = grading exponent,

and $C_i = A, \{q N_o, \epsilon^{m+1} / [(m+2)(V_d + V_r)]\}^{1/(m+2)}$ (2)

where A = area of junction,

q = charge on electron,

V_d = diffusion voltage,

V_r = reverse-bias voltage, and

$\epsilon = \epsilon_o \ \epsilon_r$ = dielectric permittivity.

S is known as a sensitivity factor or capacitance exponent[5, 6] and is equal to the gradient of the curve between $\ln C_i$ and $\ln(V_d + V_r)$ and expressed as,

$$S = -d[\ln(C_i)] / d[\ln(V_d + V_r)] \quad (3)$$

Equations (2) and (3) yield,

$$S = 1/(m+2) \quad (4)$$

In order to find out the values of S for different devices, $\ln(C_i)$ and $\ln(V_d + V_r)$ are calculated from Fig 2 and plotted in Fig 3. It is observed that the relations are nearly linear for all devices and gradients are found out to be nearly 0.5, 0.33, 1.0 for 35/0, 130/90 and 215/90 respectively. From values of S, impurity exponent m are calculated using eqn (4) and tabulated in Table 1.

Mathematical relation between the C_i and V_r is obtained by combining equations (2) and (4) as:

$$C_i = A, \{[S q N_o, \epsilon^{(1/S)-1}] / (V_d + V_r)^S\} \quad (5)$$

or

$$(1/C_i)^{1/S} = A\{[1/[S q N_o \epsilon^{(1/S)-1}]\}(V_d + V_r) \quad (6)$$

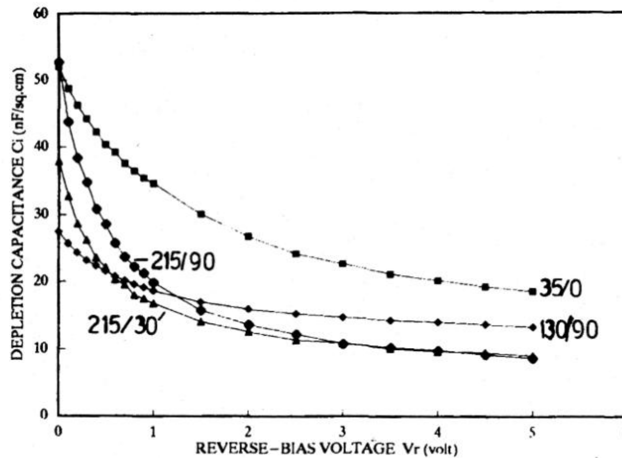

Fig 2 Relation between depletion capacitance C_i and reverse bias voltage at different thermal treatment

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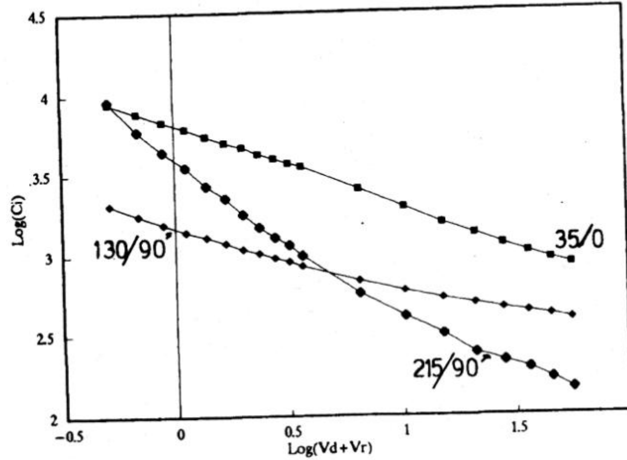

Fig 3 Log-Log plot of depletion layer capacitance *versus* reverse bias voltage at different thermal treatment. The slope indicates the sensitivity factor

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To find out the diffusion voltages (V_d) for different devices, values of $(1/C_i)^{1/S}$ are calculated from Fig 2 and Table 1; and plotted against V_r in Figs 4, 5, 6. It is observed that the plots are linear. V_d for device is obtained by interpolating the plot on abscissa and tabulated in Table 1.

In order to find out the impurity distribution from C-V plot, following method as described in [7] is used, where the charge impurity (for single sided junction and depletion region assumption), is given by,

$$N_a = 2, [C_i^3/(q, \in)] (dV_r/dC_i) \quad (7)$$

and $$W_x = \in / C_i \quad (8)$$

where W_x = position from the junction.

Values of N_a and W_x are calculated from Fig 2 for different devices and plotted in Fig 7. The junction type and impurity density, as observed from the plots are tabulated in Table 1. It is apparent from the plots that at 35°C the device junction is abrupt, at 130°C the device junction is linearly graded and at 215°C device junction becomes hyperabrupt. It is further observed that at 215°C treatment, the N_a close to junction increases with treatment time, however at $W_x > 0.8$ micron it appears to converge to $N_a = 0.5 \times 10^{15}$ without any apparent change.

Table 1 Effect of thermal treatment on various device parameters

Device	35/0	130/90	215/30	215/60	215/90
Capacitance exponent '*S*'	0.5	0.33	0.8	0.95	1.0
Impurity exponent '*m*'	0	+1	−0.75	−0.93	−1.0
V_d (volt)	0.75	0.5	0.65	0.6	0.55
$N_a \times 10^{16}$	2.85	$3/\mu$	1.2	2.0	2.5
Elect. Forming Hrs.	24	20	·4	3.25	2.5
1/*S*	2	3	approximately equal to 1		
Junction	abrupt	graded	hyperabrupt		

It is also observed that the major changes in N_a occur up to 1 micron depth. The comparison of N_a at 35°C, 130°C and 215°C treatment evolves peculiar patterns if observed at $W_x = 0.3$ micron and also at 0.8 micron. It is apparent that at $W_x = < 0.3$ micron, N_a initially reduces due to increase in temperature from 35°C (35/0) to 130°C (130/90), but on the contrary starts increasing from 130°C (130/90) to 215°C (215/30). Such change is quite opposed to normal diffusion process, since there should have been a further decrease in impurity density as per $N_a = ND - NA$ (where *ND* is donor and *NA* is acceptor impurity). However at $W_x = 0.8$ micron, N_a reduces with increase in temperature for all devices which appears to be normal. This suggests that, perhaps due to intimate contact between molten cadmium and selenium, some typical phenomenon, at 215°C might be dominating N_a distribution close to junction.

In order to find out the relation of depletion width (W_d) against V_r, values of W_d are calculated from eqn (8), where W_x (max) = W_d, and plotted in Fig 8. It is observed that at $V_r = 0$V, W_d is highest for (130/90) and lowest for (35/0). It is further observed that W_d increases superlinearly for (215/30) and sublinearly for (130/90).

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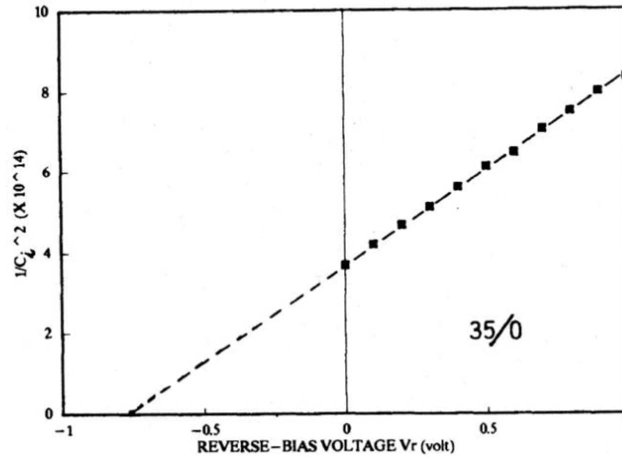

Fig 4 $1/C_i^2$ plot against reverse-bias voltage for 35/0 abrupt device to find the built-in diffusion voltage

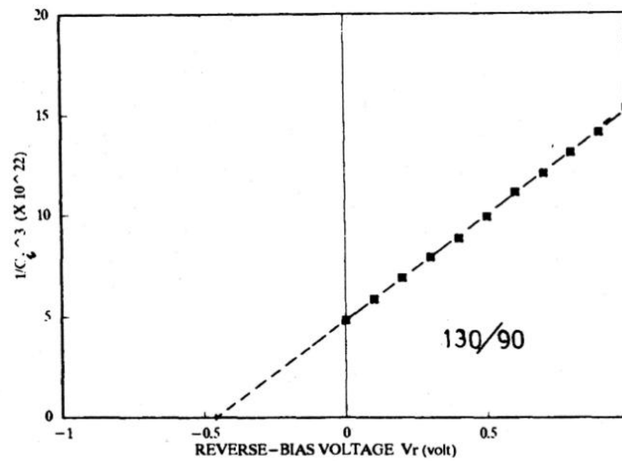

Fig 5 $1/C_i^3$ plot against reverse-bias voltage for 130/90 linearly graded device for finding diffusion voltage

The W_d curves for the devices, treated at 215°C, appear to converge at $W_d > 1$ micron.

Experimental R_d for V_r at different thermal treatment is plotted in Fig 9. It is observed that the variations of R_d with V_r is super linear at low V_r and sub linear at higher V_r. However R_d for different devices appears to decrease with increase in treatment temperature. R_d is observed to be highest for (35/0) and lowest for (215/90).

Treatment duration at 215°C appears to cause a decrease in R_d, contrary to an increase in C_i as observed Figs 9 & 2 in (215/30), (215/60) and (215/90) devices characteristics. This may be attributed to the enlargement of junction contact area at Se-Cd interface due to "wetting" of microscopic surface structure.

From dimensions of the depletion region, C_i and R_d can be calculated by assuming single sided junction and an abrupt transition between the depletion region and the adjacent neutral layer, and can be expressed as,

$$C_i = \epsilon A / W_d \qquad (9)$$

and $R_d = (1/\sigma)\ W_d / A$ (10)

By combining eqn (9) & (10) we get,

$$\sigma = \epsilon / C_i R_d \qquad (11)$$

where σ = conductivity of the region.

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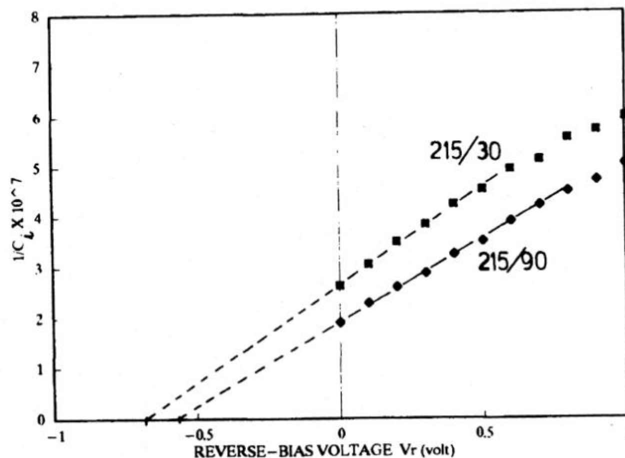

Fig 6 $1/C_i$ plot against reverse-bias voltage for 215/30 and 215/90, hyperabrupt devices, for finding V_d

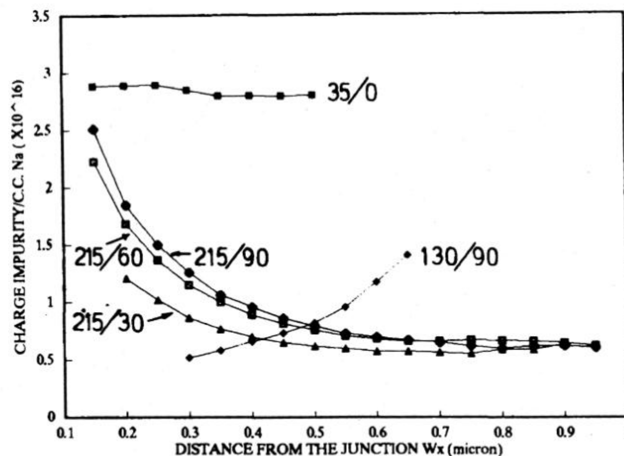

Fig 7 Impurity charge distribution near the junction for various devices as a function of distance from the junction

Conductivity σ is calculated from eqn (11), by using C_i and R_d values from Fig 2 & Fig 9 for V_r and plotted in Fig 10. It is observed that σ increases with V_r and appears to be lowest for 35/0 and highest for 215/90. It is known that conductivity depends on the mobility and density of mobile charges, and drift velocity as well as excess mobile charges both depend on the electrical field. This implies that the mobile charge density is a function of thermal treatment and V_r. The increase in mobile charges due to thermal treatment may be attributed to higher diffusion of metallic impurities (point defects) in selenium lattice. The increase of σ due to increased V_r may be attributed to higher generation of mobile charge carriers due to field.

It is known that the reverse-bias or leakage current (I_r) depends on the material and excess mobile charge generation centers in the depletion region. Number of such centers is proportional to depletion width which is again a function of voltage. The diode current can be expressed, as given in[8] as

$$I_{rg} = I_{ro} [\exp (V q / a KT) - 1] \quad (12)$$

and $$I_{ro} = q A ni W_d / 2 \tau_0 \quad (13)$$

where V = voltage across the depletion width,

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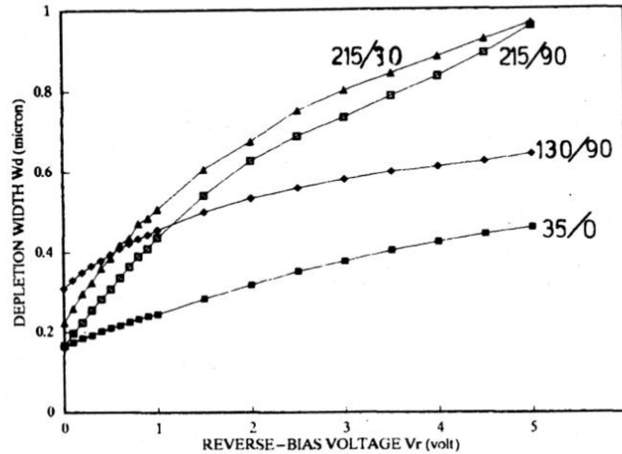

Fig 8 Effect of thermal treatment on the depletion region width (W_d) as a function of reverse bias voltage

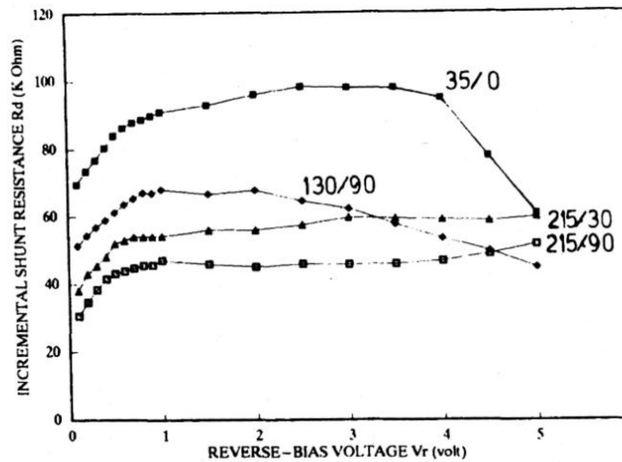

Fig 9 Variation in the incremental shunt resistance (R_d) against reverse bias voltage due to thermal treatment at different temperatures

ni = intrinsic electron concentration

I_{ro} = I_{gen} = generation current at $V = -V_r$,

τ_0 = carrier lifetime,

T = absolute temperature in Kelvin, and

K = Boltzman constant

For $V = -V_r$ and $V_r > 4KT/q$, the eqn (13) reduces to

$V_r = -I_{gen}$

Value of I_r is calculated from reverse bias voltage V_r and shunt resistance R_d, as given by,

$$I_r = V_r / R_d \quad (14)$$

and plotted in Fig 11.

It is observed that I_r increases linearly with V_r, and appears to follow eqn (13) for all devices. This further suggests that I_r is due to generation effect and not by thermal diffusion.

Effect of electrical forming on impurity distribution

Capacitance exponent S for all devices, is calculated from eqn (2) using C_i values against V_r, for before forming (BF) and after forming (AF) and plotted in Fig 12. From the comparison of the plots there does not appear to be much change in the values of S at different thermal treatment, indicating that process of electrical forming may not change the ionized impurity distribution of the devices, which is also reported elsewhere[9].

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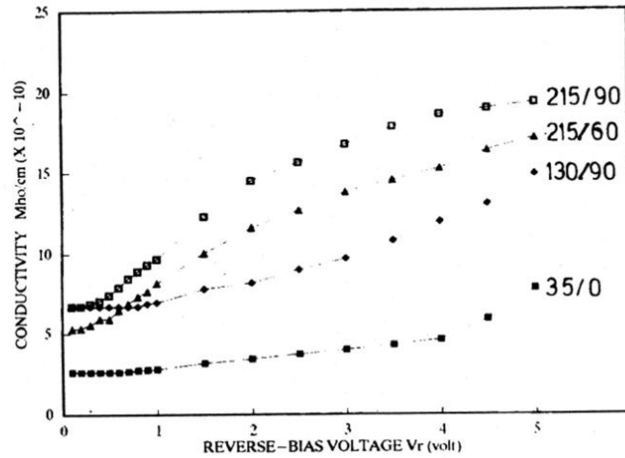

Fig 10 Variation of conductivity, computed from C_i & R_d, at different reverse-bias voltage as a function of thermal treatment

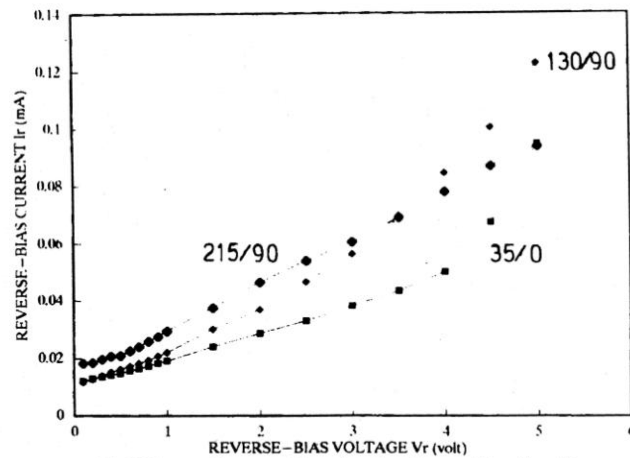

Fig 11 Reverse-bias current I_r as a function of reverse bias voltage V_r

The effect of thermal treatment on electrical forming duration

In Table 1, average forming time is shown, in hours, at 8mA/sq cm forming current, required for various devices. It is apparent from the results that the electrical forming time decreases with thermal treatment.

DISCUSSION

The effect of thermal treatment is known to influence the diffusion near the junction where the impurity density is given by the density difference of donor and acceptor (i.e., $N_a = ND - NA$). A very shallow diffusion of cadmium in uniformly doped selenium can be approximated by a one-sided abrupt junction [8]. In the present study, the 35/0 device which is treated at room temperature, leads to a diffusion which is apparent to be close to the interface thus creating an abrupt junction as shown in Fig 7.

When a junction is treated at higher temperature, it causes a higher and deeper diffusion leading to a graded distribution on semiconductor side and exponential distribution towards the metal side[8, 9]. Impurity is observed to be reducing further by 215°C treatment at $W_x > 0.8$ micron. From these observations it appears that the diffusion process is apparently involved in Se-Cd and junction behaves like a diffused junction.

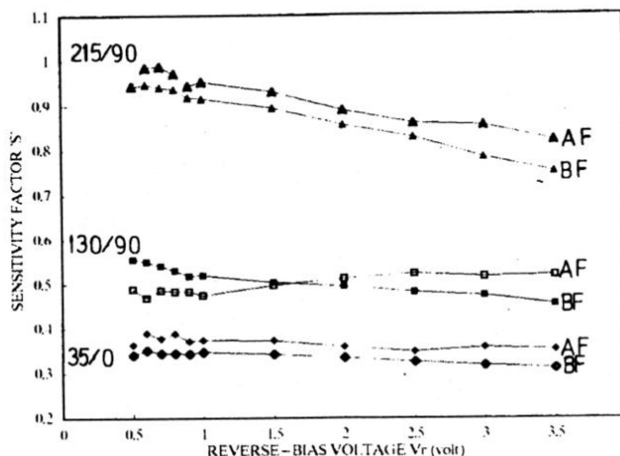

Fig 12 Comparison of the variation of capacitance exponent, before forming and after forming, against revese-bias voltage for different thermal treatments

A non-linearity of $1/C_i^2$ *versus* V_r has often been observed on polycrystalline selenium diode and has been suggested to be due to spreading of the space charge zone completely across the CdSe layer, causing a "knee" in the plot. The initial slope is reported to be due to CdSe and after the knee to the selenium as referred to by Champness in[2]. However from the present study such nonlinearity in the plot is attributed to the wrong presumption of the impurity distribution. To ascertain V_d, it has been shown that $1/C_i^2$ *versus* V_r plots are not applicable to all distributions and exponent of C_i needs to be changed to 3 and 1 for graded and hyperabrupt distribution to get linear plots.

At 215°C treatment a notable deviation in impurity distribution is observed which does not appear to be according to normal diffusion process. However this effect appears to be some what similar to the hyperabrupt device referred to in[5], wherein hyperabrupt profile is achieved by "surface trick". It appears that the surface structure of polycrystalline selenium layer created by the present process may not be perfectly smooth at microscopic level owing to surface irregularity, grain boundaries or other defects. At 215°C temperature, the molten Cd being in intimate contact, might be spreading by "wetting" process. It appears from the observations of C_i & R_d that the surface contact area at Se-Cd interface may be getting enlarged more and more with the treatment duration till there is total coverage of surface irregularity, being limited to a smaller depth.

From the present discussion and observations it appears that selenium and cadmium diode can be fabricated to have different charge profiles by suitable temperature treatment. The hyperabrupt profile appears to be unique to the present device where by treatment at 215°C, capacitance exponent to the tune of 1 can be achieved. Further work needs to be done to increase the exponent value, perhaps, by suitable surface treatment of selenium.

Further to the findings of the same authors[10], it is observed that electrical forming does not change the impurity distribution irrespective of its profile.

CONCLUSIONS

The thermal treatment changes the impurity distribution from abrupt at room temperature to graded at 130° C, and further to hyperabrupt at 215°C with capacitance exponent of 0.5, 0.33 and 1.0 respectively. The duration of thermal treatment at 215°C appears to enlarge the surface contact area due to higher wetting of the molten Cadmium at Cd-Se interface thus creating a hyperabrupt profile. The capacitance exponent could possibly be increased to more than 1, by suitable surface treatment, however it requires further investigation. The electrical forming does not affect the immobile impurity distribution and forming duration depends on the preceding thermal treatment.

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