27th International Symposium on Compound Semiconductors

2 - 5 October 2000

27 July 2000

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Dear Dr. Ingole,

Your paper as been accepted for oral presentation at the 27th International Symposium on Compound Semiconductors. The conference will be held on 2 - 5 October 2000 at the Hyatt Regency Monterey, Monterey, CA.

Session:	TuD: Characterization III
Paper Title:	Effect of Interlayer Insulation of CdSe Junction Capacitance under Reserve Bias
Date:	Tuesday, 3 October 2000
Time:	3:50 PM - 4:10 PM

The exact location of your presentation will be listed in the Advance Program. You will receive a copy as soon as it becomes available. **The time allocated for your talk is 20 minutes, inclusive of questions and answers.** An overhead projector, screen, pointer and microphone will be available during your presentation. If you require additional audio visual equipment, please fill out and fax the enclosed request form.

At this time you should prepare your final manuscript for publication in the Technical Proceedings Digest, which will be distributed at the conference. Your final manuscript should be a maximum of six typed pages, single spaced on 8.5" x 11" white paper, if you prefer you may use the enclosed galley sheets. For your convenience, I have enclosed an author kit containing the Manuscript Preparation Instructions and several Galley Sheets.

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All speakers, chairpersons and committee members are required to pay the registration fee in order to support the conference. Complete registration information will be sent to you with a copy of the Advance Program. Thank you for your support of ISCS 2000. I look forward to seeing you in Monterey.

Sincerely,

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Effect of Interlayer Insulation on CdSe Junction Capacitance under Reverse Bias

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Abstract. CdSe devices were fabricated in batches by laying interlayer insulation of different thickness between cadmium and selenium layers. The manifestations of such insulation thickness on device capacitance and shunt resistance under reverse bias condition are investigated. It is reported that insulation does not affect the impurity profile. Device simulation with experimental verification is presented.

1. Introduction

Selenium cadmium junction was firstly reported by F. Braun in 1874. Selenium Cadmium device is commercially known as selenium rectifier or diode. Such diodes are used in battery chargers, electroplating supply, alternator excitation system, extra high tension supply of television, Xeroxing machine, photo-sensitive devices, varactors [1] etc. Cadmium (Cd) and Selenium (Se) junction is basically a low voltage device. Various manufacturing processes have been suggested to improve its reverse voltage performance. The reverse bias voltage characteristic can be improved by applying an interlayer insulation between Cd and Se during fabrication. Such an improved device is called a double voltage rectifier [2, 3]. The authors have undertaken a comprehensive study of such a device. The effect of electrical and thermal treatment on CdSe diode has already been reported [1]. The present work further investigates the effect of different thickness of interlayer insulation on the device capacitance and resistance under reverse bias condition. This investigation is divided in the following areas: i) the charge impurity density, ii) capacitance, iii) resistance, and iv) effect of electrical forming on device capacitance.

2. Fabrication

The present devices were fabricated by vacuum deposition technique as described in [1,3]. Uniform interlayer insulation was applied between Cd and Se during fabrication by solvent spray techniques. For the sake of comparison, overall insulation thickness is gauged in terms of number of layers. The desired thickness was achieved by varying number of such layers during the fabrication. The insulation material was a solution of Shellac and Gun Cotton in acetone [4]. In the present study, device samples having 1, 2, 3, and 4 layers were fabricated in batches of twenty devices each, however the first batch

was fabricated without such insulation. To minimise the effect of process variations and material on the device parameters, they were processed in batches. Ten devices each of 1 cm^2 area from every batch were selected for the present studies and average performance is presented. The devices having 0, 1, 2, 3, and 4 layers are labelled as LC0, LC1, LC2, LC3, and LC4 respectively.

3. Measurements and Results

In order to improve the diode performance under reverse bias condition, it is necessary to form the device by passing rectified alternating current in the reverse direction for certain time duration [1,3], which is known as *Electrical Forming*. To compare the effect of electrical forming, two sets of measurement are taken on the same device before electrical forming (*BF*) and after electrical forming (*AF*). For the analysis, various measurements of electrically formed devices are considered. The device capacitance (C_i) and shunt resistance (R_d) are measured with the help of a capacitance bridge at different reverse bias voltages (V_r). Due care is taken to perform the measurements in shortest possible time to avoid DC creep [3].

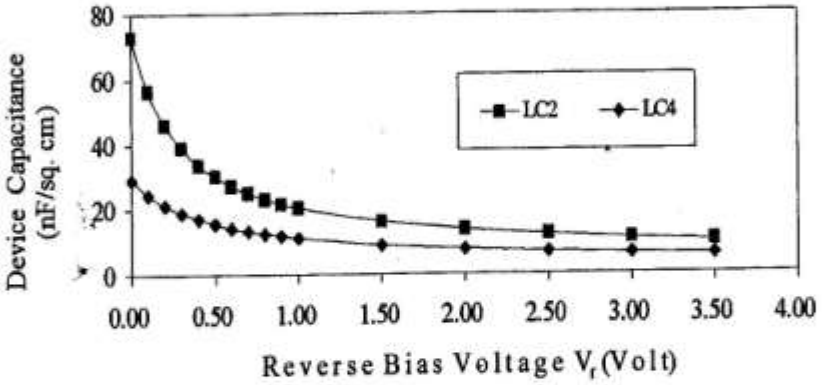

Figure 1

The relations between C_i against V_r are plotted for different devices in Fig. 1. It is observed that C_i decreases with V_r. It is further observed that higher insulation thickness (due to more insulation layers) cause decease in C_i. For studying the effect of insulation thickness on charge impurity profile, the impurity exponent (m) of various devices, impurity distribution (N_a) in the depletion region are calculated by using *Power Law* [1,5]. The m of all devices are calculated from the ratios of $ln(C_i)$ and $ln(V_r + V_d)$. It is found that the value of m is close to unity at different V_r for all devices.

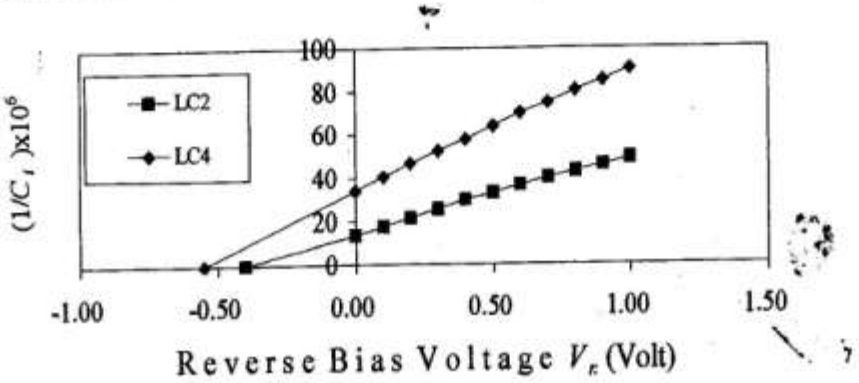

Figure 2

Diffusion voltages (V_d) of various devices at m=1 are found out by plotting $1/C_i$ and V_r relation in Fig. 2. All relations are observed to be straight lines. However, V_d is found to be 0.4 V for LC2 and 0.55 V for LC4. It appears that V_d marginally increases with insulation thickness.

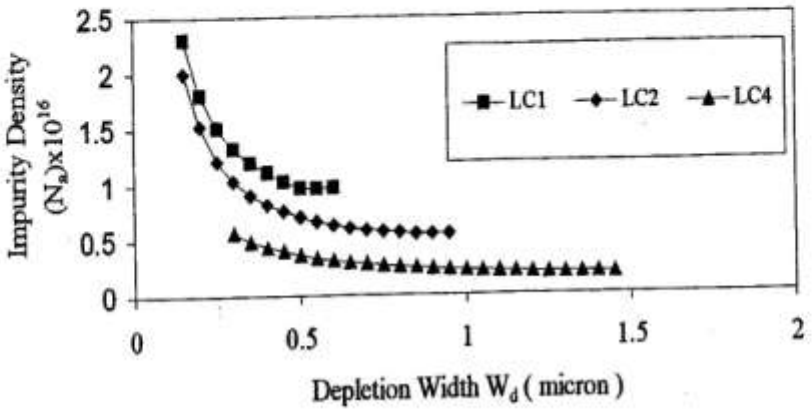

Figure 3

A method as described in [6] is implemented for the evaluation of N_a from *capacitance-voltage* (C-V) plot by assuming the validity of complete depletion approximation. N_a and depletion width (W_d) are evaluated from C_b and plotted in Fig. 3. From the nature of the charge impurity distribution, it is observed that the present devices are hyperabrupt [1]. N_a characteristics shift continually downwards with increase in interfacial insulation thickness. The shift in N_a could be attributed to the effect of insulation therefore calculated N_a may not be the actual charge impurity density associated with the junction.

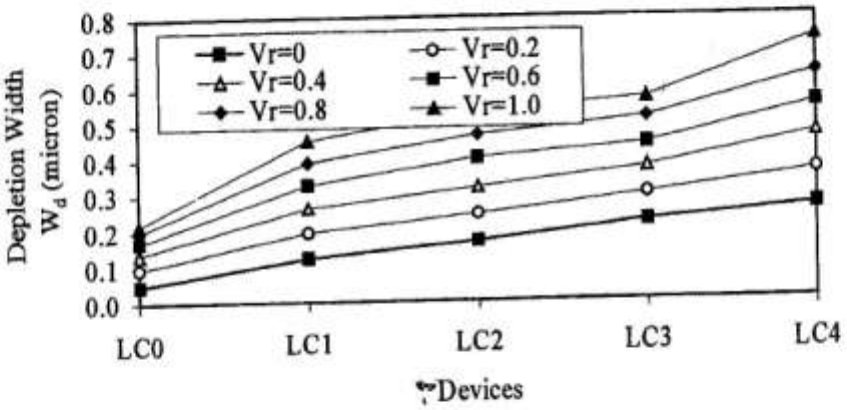

Figure 4

To establish a relation between insulation thickness and device capacitance, initially the test values of C_i of *BF* devices are only considered to avoid any likely influence of the electrical forming on the junction geometry and parameters. W_d is calculated [1] from experimental C_i (*BF*) at different values of V_r. For same value of V_r corresponding values of W_d are tabulated for LC0, LC1, LC2, LC3, and LC4 devices and repeated for different V_r. Relations of W_d and respective devices are plotted in terms of number of layers at different Vr in Fig. 4. It is observed that W_d increases linearly with insulation layers at V_r = 0. However, for higher values of V_r, there are deviations.

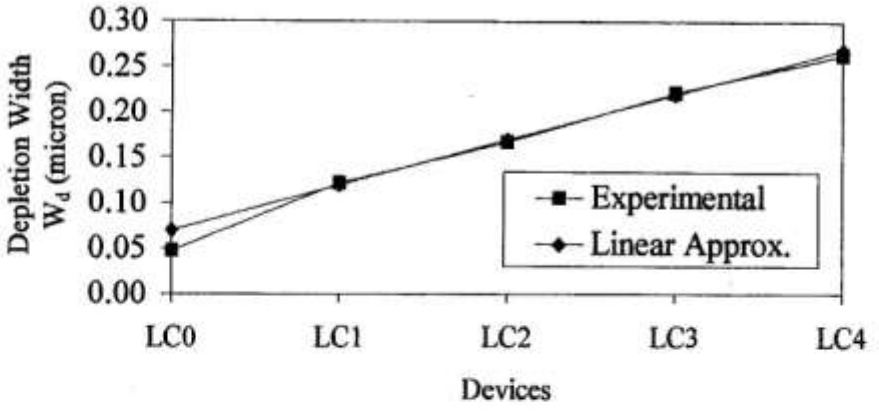

Figure 5

To investigate the constituents of device capacitance, relation between W_d and number of insulation layers at $V_r = 0$ are considered. The relation between W_d and insulation layer at $V_r = 0$ is plotted and approximated by a straight line as shown in Fig. 5 and equation of depletion width for n layers (W_n) can be expressed as

$$W_n = 0.05n + 0.07 \qquad (1)$$

Intercept in micron on W_d axis at $V_r = 0$ for LC0 and slope (micron/insulation layer) are taken as 0.07 and 0.05, respectively. It is obvious from this equation that calculated junction width from C_i measurement comprises a transition region width (given by the intercept on Y-axis) and insulation width. The relation (1) transforms further in terms of capacitance

$$\frac{1}{C_i} = \frac{kn}{C_l} + \frac{1}{C_s} \qquad (2)$$

where k is a relative constant due to materials , C_l is insulation capacitance/layer, and C_s *is* transition region capacitance. The validity of (2) is established by simulating a capacitance characteristic of (AF) devices LC2 from LC3.

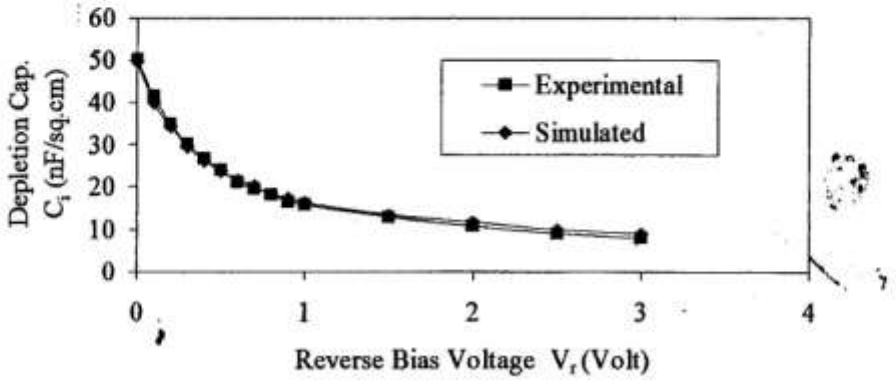

Figure 6

Simulated and experimental characteristics of LC2 are plotted in Fig. 6. It is observed that both C-V curves are cognate. This establishes that the constants of (1) and (2) are not affected by electrical forming as initially considered.

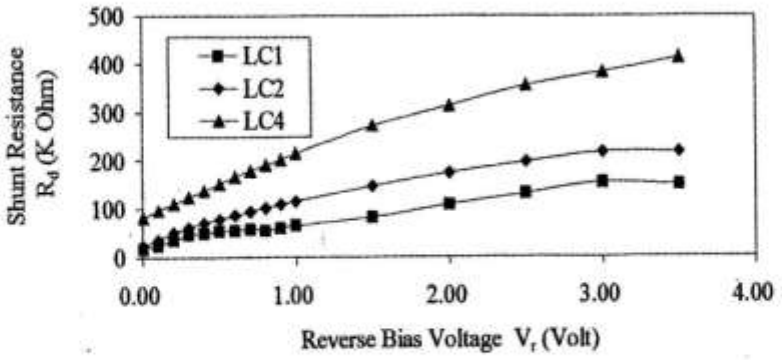

Figure 7

The experimental values of device shunt resistance (R_d) against V_r are plotted in Fig. 7 for LC2, LC3 and LC4. It is observed that R_d increases with increase in V_r. It is further observed that R_d increases continually with increase in insulation thickness. Conductivity (σ) of the reverse bias region is calculated from the relation of R_d and C_i and is given by [5,6],

$$\sigma = \frac{Ci\, R_d}{\varepsilon} \qquad (3)$$

where ε is permittivity.

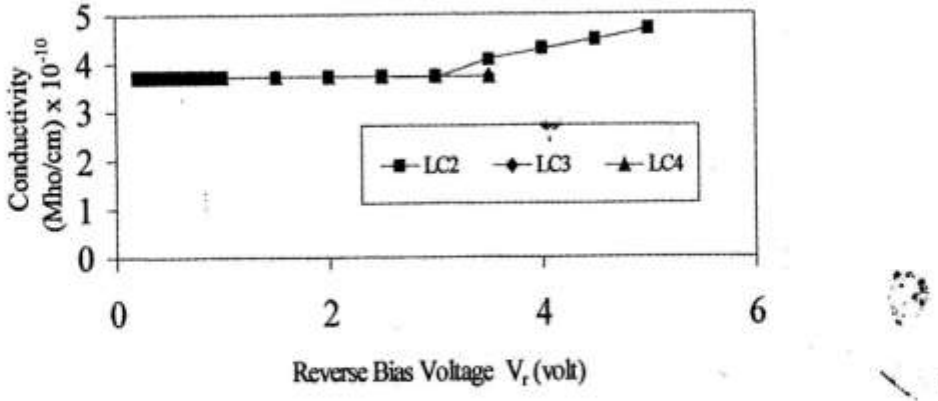

Figure 8

σ is plotted against V_r in Fig. 8. It is observed that at lower V_r, σ of various devices are congruent. It is further observed that LC3 and LC4 have the lowest conductivity. This suggests that conductivity is rendered unaffected beyond certain insulation thickness.

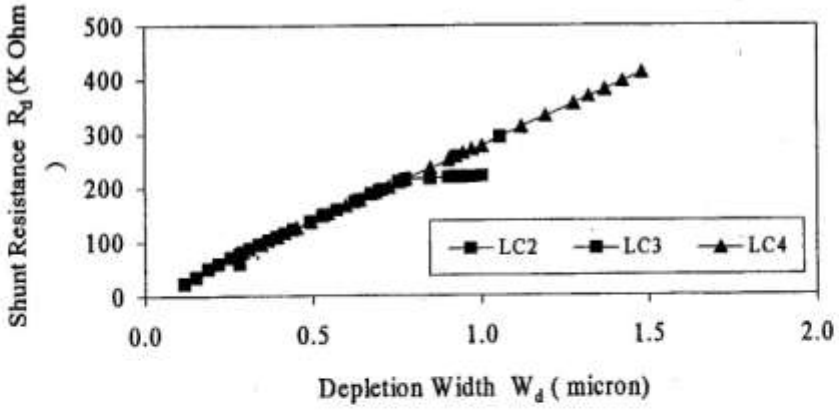

Figure 9

The relationship between R_d and W_d is found out by plotting R_d against W_d for devices LC2, LC3, and LC4 in Fig. 9. It is observed that various characteristics are congruent and varies linearly. The relation can be simulated by a straight line and expressed in terms of an equation

$$R_d = 2975 W_d \qquad (4)$$

where R_d is in kilo ohms and W_d is in micron.

4. Conclusions

The device capacitance consists of two basic constituents, namely transition region capacitance and insulation capacitance acting in series. The value of insulation capacitance decreases with increase in insulation thickness. Insulation capacitance is not affected by electrical forming. The variation of insulation thickness does not affect the junction profile. A device capacitance and resistance can be simulated by established reactions. Diffusion voltage marginally increases with increased insulation thickness. It is shown that the conductivity of depletion region becomes more consistent due to the higher insulation thickness.

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