New technique for quadrilateral distance relay

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ABSTRACT

A new technique for the development of a quadrilateral distance relay for transmission-line protection is reported. The modus operandi consists in continuously monitoring the coincidence period of four suitably derived relaying quantities, and the relay is made to develop trip output if the coincidence period is zero, whereas if the coincidence period is finite, the relay develops restraining output. Such a simple criterion results in extreme simplicity of the relay circuitry.

LIST OF SYMBOLS

S_1, S_2, S_3 and S_4 = relaying inputs
Z_a, Z_b and Z_c = replica impedances defining the vertices of the quadrilateral
Z_r = V_r/I_r = impedance seen by the relay
V_r = voltage at the relay location
I_r = current at the relay location

1 INTRODUCTION

The rapid growth of power systems owing to increasing demand, as well as interconnections, has resulted in e.h.v. lines being used over longer distances to deliver the bulk of the power. However, such long and heavily loaded lines demand that greater attention be paid to the problems arising out of the encroachment of the loci of maximum load and power swings into the distance-relay characteristic. Attempts to overcome these problems have resulted in the quadrilateral characteristic, which fits the fault characteristic of the transmission line fairly well.

Although numerous techniques[1-7] have been reported for developing such a characteristic, most of them either require larger numbers of relaying inputs and/or quite an elaborate circuit. The new technique that is reported here required four relaying inputs and an extremely simple circuit.

2 SUGGESTED TECHNIQUE

2.1 Relaying quantities

The desired quadrilateral characteristic, defined by the extremities of phasors Z_a, Z_b and Z_c, is shown in Fig. 1A, whereas Fig. 1B shows the relaying quantities for any relay impedance phasor Z_r, defined by point P_1.

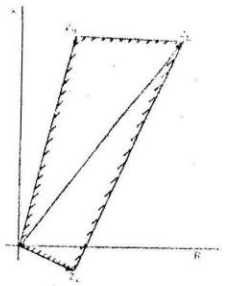

Fig 1A

Quadrilateral polar characteristic

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The relaying quantities are thus defined as

S_1 : Z_a Z_r $I_r \cdot Z_a$ V_r
S_2 : Z_b Z_r $I_r \cdot Z_b$ V_r
S_3 : Z_c Z_r $I_r \cdot Z_c$ V_r
S_4 : Z_r V_r

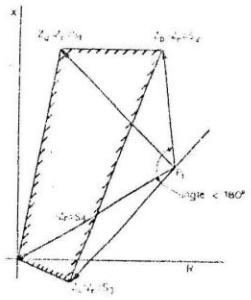

Fig. 1B

Relaying quantities

2.2 Properties of relaying inputs in trip and restraining region

In Fig. 1B, the relay impedance phasor Z_r, defined by point P_1, is shown in the restraining region. Observing the phasor dispositions of the relaying quantities S_1 to S_4, the following general conclusion is drawn:

'Whenever the relay impedance phasor Z_r is in the restraining region, all the relaying phasors are confined to 180° phase-angle margin.

Fig. 2 shows the relay impedance phasor Z_r, defined by point P_2 as crossed over into the trip region. The conclusion relating to the phasor dispositions of relaying quantities S_1-S_4 is now found to be:

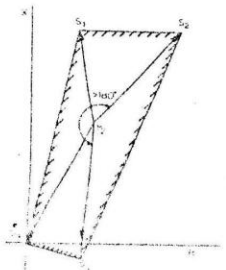

Fig. 2

Phasor dispositions of S_1-S_4 for Z_r in trip region

'Whenever the relay impedance phasor Z_r is in the trip region, all the relaying phasors are confined to more than 180° phase-angle margin'

2.3 Coincidence periods of relay inputs in restraining and trip region

Figs. 3A and B show, respectively, the relay phasor positions as confined to 180° phase-angle margin (for Z_r in restraining region), and confined to more than 180° phase-angle margin (for Z_r in trip region). The conclusions with regard to their coincidence period are as follows:

(a) In the restraining region, the coincidence period is finite and is governed by two extreme phasors.
(b) In the tripping region, the coincidence period is zero or there is no coincidence period.

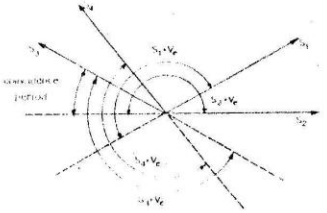

Fig. 3A

Finite coincidence period for phasors confined to less than 180° phase-angle margin

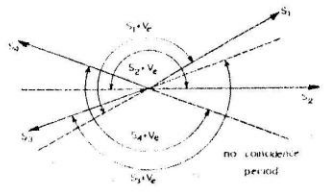

Fig. 3B

Zero coincidence period for phasors confined to more than 180° phase-angle margin

2.4 Principle and block diagram of relay

Fig. 4 shows the complete block diagram of the relay

The relaying inputs S_1-S_4 are derived as functions of V_r and I_r, with the help of replica impedances Z_a, Z_b and Z_c and a potential transformer.

These inputs are then fed to a coincidence gate, which delivers output pulses periodically, every 20 ms, based on a power frequency of 50 Hz, for Z_r in the restraining region. The pulse stretcher, which is a 20 ms monostable triggering on the leading edge of the input pulses, delivers continuous output to energise a slave relay having normally closed contacts. The contacts are thus kept open for Z_r in the restraining region.

Whenever Z_r falls in the tripping region owing to fault conditions on the line, the coincidence gate, and thus the pulse stretcher, delivers no output, resulting in the drop out of the slave relay. The slave relay, therefore, closes its contact as an indication of trip output.

3 PROTOTYPE RELAY

The circuit arrangement of the relay unit based on the above principle is shown in Fig. 5.

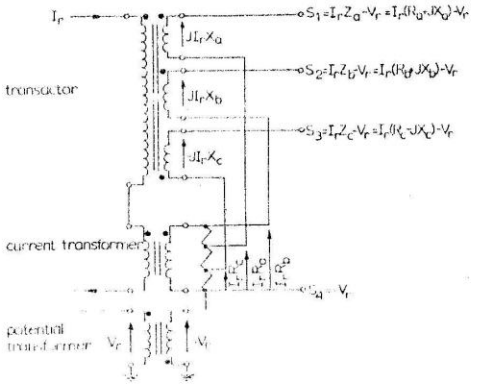

Fig. 5A

Derivation of relaying inputs

Fig. 5A shows how the four relaying inputs S_1-S_4, as functions of V_r and I_r, are derived with the help of a transactor, an auxiliary current transformer and an auxiliary potential transformer, whereas Fig. 5B shows the transistor circuitry consisting of four clippers, a NAND gate, a monostable as a 20 ms pulse stretcher and the slave relay (reed type).

4 EXPERIMENTAL RESULTS

The static polar characteristic is shown in Fig. 6A, for a constant value of I_r equal to 1·0 A.

Accuracy/range characteristics for steady-state and fully offset conditions of the relay current are shown in Fig. 6. The relay operated within an accuracy of 10% up to a range of 30, and the maximum transient overreach was found to be 7%.

The operating time was found to vary from instantaneous to a maximum of one cycle (20 ms) depending on the instant of fault.

The burden of potential circuit and the current circuit was found to be 0·4 VA and 0·5 VA, respectively.

5 CONCLUSIONS

A novel technique has been presented for developing a quadrilateral distance relay, requiring four suitably derived

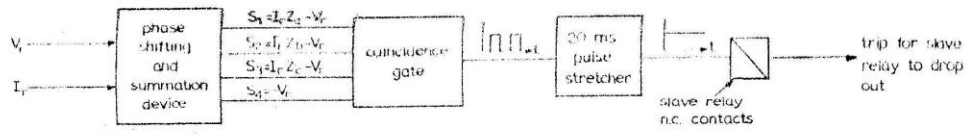

Fig. 4

Block diagram of relay

relaying inputs, followed by a very simple circuitry, the modus operandi of the relay being the generation of trip output if the coincidence period of the four relaying quantities is zero.

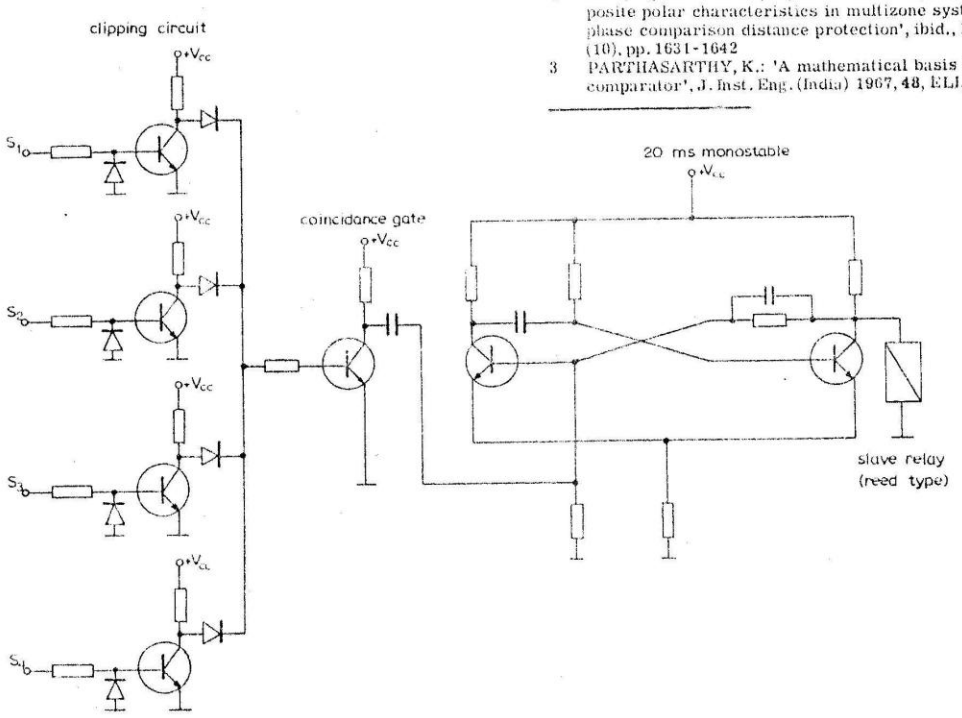

Fig. 5B

Relay circuitry

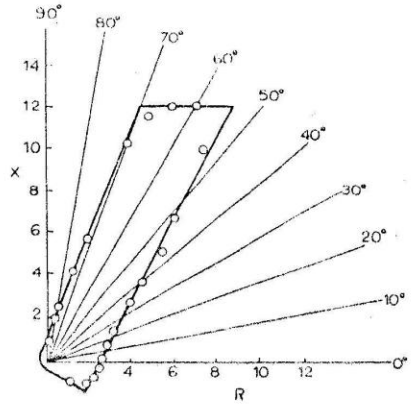

Fig. 6A

Static polar characteristic at constant $I_r = 1{\cdot}0\,A$

The experimental results show quite satisfactory performance with respect to the operating range, transient overreach, VA burden and the operating time, except that the relay, in the present form, tends to maloperate when not energised, i.e. in the absence of basic relaying inputs I_r and V_r. This difficulty is being overcome by providing a suitable bias to the slave relay, derived from the output of a NAND gate, supplied with the rectified (fullwave) relay inputs I_r and V_r. This arrangement further ensures the correct directional feature for the relay by positively excluding the origin of the R/X diagram from the trip region of the relay.

6. REFERENCES

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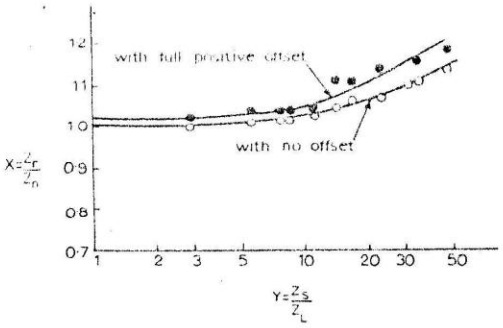

Fig. 6B

Accuracy versus range characteristics

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